Refine Search

Search Results -

Terms	Documents
(socket or slot) same (configur$5 near5 bus) same indicator	6

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L3

Refine Search

Recall Text Clear Interrupt

Search History

DATE: Monday, June 28, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT,USOC; PLUR=YES; OP=OR			
L3	(socket or slot) same (configur$5 near5 bus) same indicator	6	L3
L2	socket same slot same (configur$5 near5 bus) same indicator	0	L2
L1	(socket near10 slot) same (configur$5 near5 bus) same indicator	0	L1

END OF SEARCH HISTORY

h e b b cg b e e ch

Refine Search

Search Results -

Terms	Documents
L3	0

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L4

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Monday, June 28, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
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L4	L3	0	L4
DB=USPT,USOC; PLUR=YES; OP=OR			
L3	(socket or slot) same (configur$5 near5 bus) same indicator	6	L3
L2	socket same slot same (configur$5 near5 bus) same indicator	0	L2
L1	(socket near10 slot) same (configur$5 near5 bus) same indicator	0	L1

END OF SEARCH HISTORY

h e b b cg b e e ch

Refine Search

Search Results -

Terms	Documents
(439/43 |439/55 |439/928.1 |361/683 |361/686 |361/600 |361/636 |361/748 |361/760 |361/736 |710/301 |710/2 |710/105 |710/8 |710/100 |710/10 |710/104 |710/11 |710/305 |710/62 |713/300 |713/100 |326/63).ccls.	11768

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L5

Refine Search

Recall Text Clear Interrupt

Search History

DATE: Monday, June 28, 2004 Printable Copy Create Case

Set Name side by side	Query
	DB=USPT,USOC; PLUR=YES; OP=OR
L5	710/301,2,105,8,100,10,104,11,305,62;361/683,686,600,636,748,760,736;439/43,55,928.1;326/6
	DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR
L4	L3
	DB=USPT,USOC; PLUR=YES; OP=OR
L3	(socket or slot) same (configur$5 near5 bus) same indicator
L2	socket same slot same (configur$5 near5 bus) same indicator
L1	(socket near10 slot) same (configur$5 near5 bus) same indicator

END OF SEARCH HISTORY

h e b b cg b e e ch

Refine Search

Search Results -

Terms	Documents
L5 and L6	16

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L7

Refine Search

Recall Text Clear Interrupt

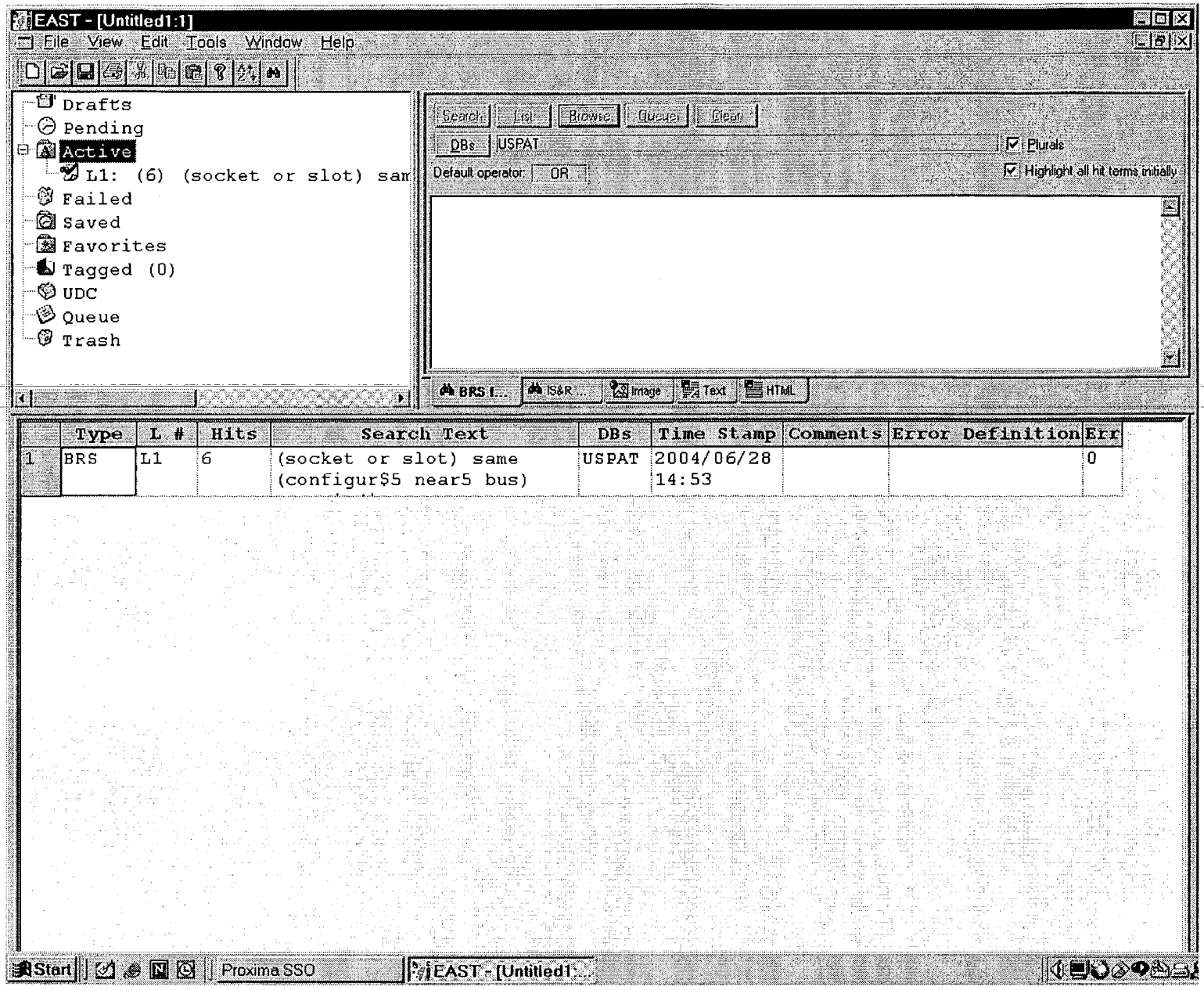
Search History

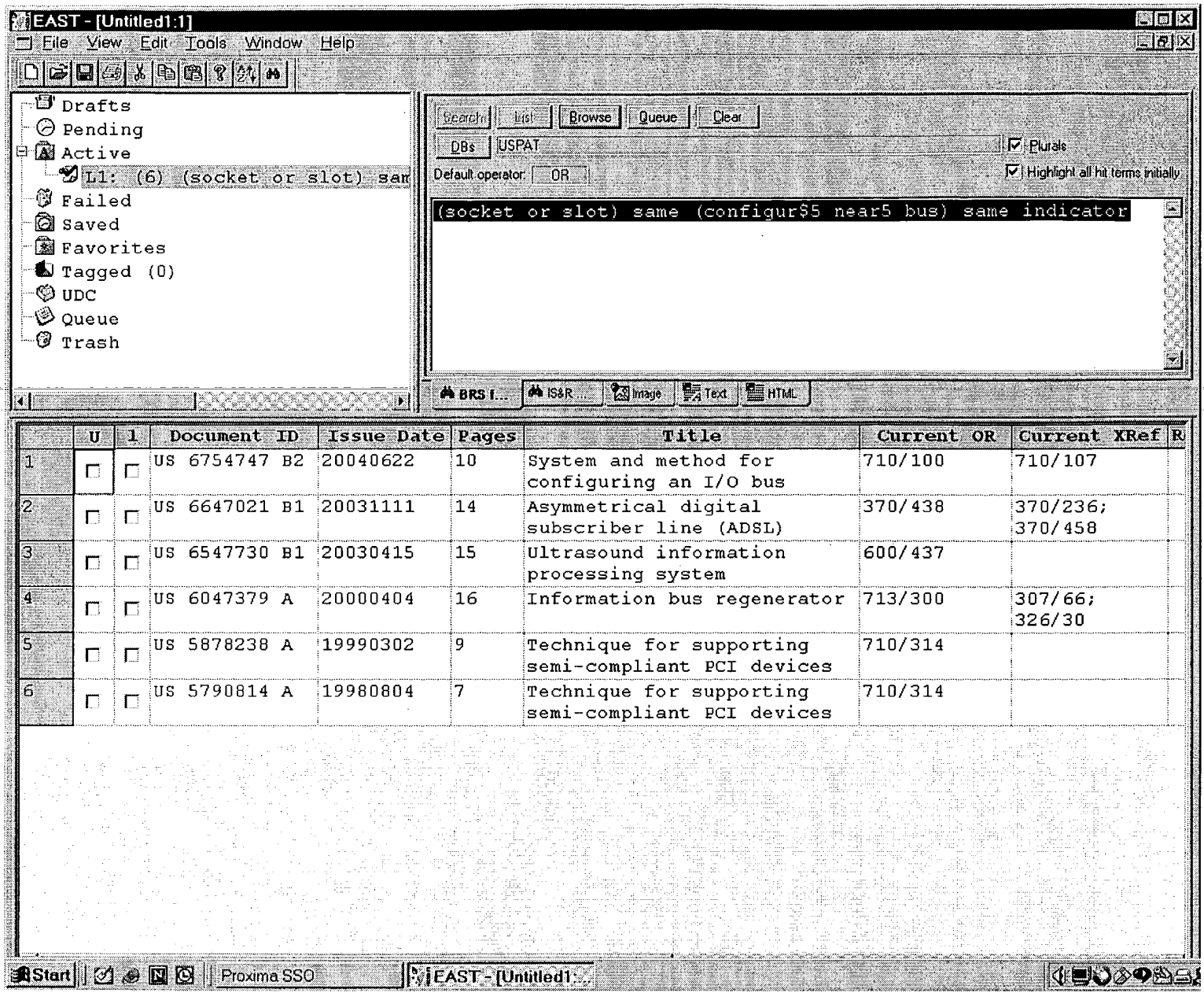
DATE: Monday, June 28, 2004 Printable Copy Create Case

Set Name side by side	Query
	DB=USPT,USOC; PLUR=YES; OP=OR
L7	l5 and L6
L6	(configur$5 near5 bus) same indicator
L5	710/301,2,105,8,100,10,104,11,305,62;361/683,686,600,636,748,760,736;439/43,55,928.1;326/6
	DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR
L4	L3
	DB=USPT,USOC; PLUR=YES; OP=OR
L3	(socket or slot) same (configur$5 near5 bus) same indicator
L2	socket same slot same (configur$5 near5 bus) same indicator
L1	(socket near10 slot) same (configur$5 near5 bus) same indicator

END OF SEARCH HISTORY

h e b b cg b e e ch


EAST - [Untitled1:1]
File View Edit Tools Window Help
Drafts
Pending
Active
L1: (6) (socket or slot) sam
Failed
Saved
Favorites
Tagged (0)
UDC
Queue
Trash
Search List Browse Queues Clear
DBs USPAT
Plurals
Default operator: OR
Highlight all hit terms initially
BRS I... IS&R... Image Text HTML
Type L # Hits Search Text DBs Time Stamp Comments Error Definition Err
1 BRS L1 6 (socket or slot) same (configur$5 near5 bus) USPAT 2004/06/28 14:53 0
Start
Proxima SSO
EAST - [Untitled1:...



	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	R
1	☐	☐	US 6754747 B2	20040622	10	System and method for configuring an I/O bus	710/100	710/107	
2	☐	☐	US 6647021 B1	20031111	14	Asymmetrical digital subscriber line (ADSL)	370/438	370/236; 370/458	
3	☐	☐	US 6547730 B1	20030415	15	Ultrasound information processing system	600/437		
4	☐	☐	US 6047379 A	20000404	16	Information bus regenerator	713/300	307/66; 326/30	
5	☐	☐	US 5878238 A	19990302	9	Technique for supporting semi-compliant PCI devices	710/314		
6	☐	☐	US 5790814 A	19980804	7	Technique for supporting semi-compliant PCI devices	710/314		

Your search matched **5** of **1047691** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance Descending** order.

Refine This Search:
You may refine your search by editing the current search expression or enter new one in the text box.

(socket or slot) and configur* and bus and (card or b Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

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1 **A new CAMAC and VXIbus high performance highway interconnect**
Cleary, R.T.;
Nuclear Science, IEEE Transactions on , Volume: 44 , Issue: 3 , June 1997
Pages:393 - 397

[Abstract] [PDF Full-Text (564 KB)] **IEEE JNL**

---

2 **A new CAMAC and VXIbus high performance highway interconnect**
Cleary, R.T.;
Nuclear Science Symposium, 1996. Conference Record., 1996 IEEE , Volume: 1 , 2-9 Nov. 1996
Pages:460 - 464 vol.1

[Abstract] [PDF Full-Text (504 KB)] **IEEE CNF**

---

3 **The design of a PC-based, low-cost radar video signal generator**
Olsen, D.W.; Willis, M.J.;
Aerospace and Electronics Conference, 1997. NAECON 1997., Proceedings of IEEE 1997 National , Volume: 2 , 14-17 July 1997
Pages:544 - 551 vol.2

[Abstract] [PDF Full-Text (640 KB)] **IEEE CNF**

---

4 **PC/104-ISA to PCI**
Brown, M.F.;
WESCON/98 , 15-17 Sept. 1998
Pages:210 - 215

[Abstract] [PDF Full-Text (776 KB)] **IEEE CNF**

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5 **A PC based voice mailing system**
Pande, A.; Sirkar, K.; Kanade, A.; Gracias, P.; Pandit, N.; Kumar, K.R.; Krishnamachari, H.;
TENCON '89. Fourth IEEE Region 10 International Conference , 22-24 Nov. 19
Pages:503 - 506

[Abstract] [PDF Full-Text (288 KB)] **IEEE CNF**

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PC/104-ISA to PCI

Brown, M.F.
Adastra Syst. Corp., Hayward, CA, USA ;

This paper appears in: **WESCON/98**

Meeting Date: 09/15/1998 - 09/17/1998
Publication Date: 15-17 Sept. 1998
Location: Anaheim, CA USA
On page(s): 210 - 215
Reference Cited: 7
Number of Pages: iv+366
Inspec Accession Number: 6201144

Abstract:
Describes the PC/104 standard. PC/104 is simply the ISA **bus** packaged in a s pin and **socket configuration**. This form-factor is ideal for embedding into e It does not rely on a backplane or motherboard architecture to interconnect tl **bus**. In a stack of one or two **boards**, the system designer can satisfy all his requirements. The final product can be considerably smaller than a standard I more reliable mounting and connectors it is able to work in more demanding environments

Index Terms:
electric connectors standards system buses ISA **bus** PC/104 standard connectors stackable pin and **socket configuration** system **bus**

Documents that cite this document
There are no citing documents available in IEEE Xplore at this time.

Search Results [PDF FULL-TEXT 776 KB] PREV NEXT DOWNLOAD CITATION

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Your search matched **0** of **1047691** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance** **Descending** order.

Refine This Search:
You may refine your search by editing the current search expression or enter new one in the text box.

(socket or slot) and configur* and bus and indicator Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

Results:
No documents matched your query.

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First Hit Fwd Refs

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L3: Entry 1 of 6 File: USPT Jun 22, 2004

DOCUMENT-IDENTIFIER: US 6754747 B2
TITLE: System and method for configuring an I/O bus

Abstract Text (1):
A system and method are provided for configuring an I/O bus. The system and method includes a plurality of adapter cards. A plurality of adapter card slots associated with the I/O busses receive the adapter cards into the computer. A user initiates optimization to check for configuration optimization problems and more specifically to check the placement of the adapter cards within the adapter card slots of the I/O busses. The user initiates optimization and in turn activates the improvement engine within the computer. The improvement engine analyzes the data transfer rates of the I/O busses and adapter cards and the placement of the adapter cards to determine an improved configuration of the adapter cards within the I/O busses. Indicators located proximate to the I/O busses display visual indication regarding the adapter card placement within the I/O busses allowing the user to determine if the configuration can be improved.

Brief Summary Text (14):
In accordance with one aspect of the present disclosure, a system and method provides visual indication of I/O bus configuration optimization problems and solutions. A computer has a plurality of adapter cards. A user inserts the adapter cards into adapter card slots interfaced with the I/O busses of the computer. The user presses an optimization switch, located on the computer, to check the current adapter card configuration. Pressing the optimization switch activates an improvement engine within the computer to analyze the I/O busses and the adapter cards to determine an improved configuration of the adapter cards within the adapter card slots of the I/O busses. Indicators located on the computer and proximate to the adapter card slots display visual indication on whether or not the adapter card placement within the I/O busses is an optimal configuration.

Brief Summary Text (18):
Another important technical advantage of the present disclosure is that it simplifies servicing by telephone. If a technical support staff suspects that an I/O bus adapter card slot configuration problem causes a user's overall problem, the technical support staff can tell the user to activate optimization and the user can quickly report back to the technical support staff what the indicators display. The technical support staff can determine if there is an optimization configuration problem from what the indicators display. Therefore, users unaware of configuration problems, adapter cards, and I/O busses and having problems associated with any of these items can have these problems adequately addressed with servicing over the telephone.

Detailed Description Text (9):
Indicators 116 denote four different states in relation to adapter card slots 108. Indicator 116 unlit indicates that no adapter card is present within adapter card slot 108. Indicator 116 that is a steady green indicates that adapter card 110 located in adapter card slot 108 does not limit the data transfer rate. Indicator 116 flashing amber indicates that adapter card 110 located in that adapter card slot 108 limits the bus transfer rate causing the configuration to not be optimized. Indicator 116 flashing green gives the indication of where the adapter

card 110 limiting the configuration should be moved in order to improve the data transfer rate.

CLAIMS:

20. A method for improving an adapter card configuration within a plurality of I/O busses, the method comprising: adding an adapter card to the I/O busses; initiating a performance check; reading indicators to ascertain if the adapter card configuration is limiting the data transfer rate; moving an adapter card from a non-optimal adapter card slot location to a suggested improved adapter card slot location to improve the adapter card configuration to improve I/O bus performance.

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L3: Entry 1 of 6 File: USPT Jun 22, 2004

US-PAT-NO: 6754747
DOCUMENT-IDENTIFIER: US 6754747 B2

TITLE: System and method for configuring an I/O bus

DATE-ISSUED: June 22, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Locklear; David A.	Austin	TX		
Wright; Michael A.	Round Rock	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Dell Products L.P.	Round Rock	TX			02

APPL-NO: 09/ 769799 [PALM]
DATE FILED: January 25, 2001

INT-CL: [07] G06 F 13/00

US-CL-ISSUED: 710/100; 710/107
US-CL-CURRENT: 710/100; 710/107

FIELD-OF-SEARCH: 710/47, 710/33-52, 710/57, 710/58, 710/109, 710/100, 710/107, 710/113, 710/154, 710/323, 710/305, 713/2, 713/600

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5179670	January 1993	Farmwald et al.	395/325
☐	5329621	July 1994	Burgess et al.	395/325
☐	5465346	November 1995	Parks et al.	395/296
☐	5533205	July 1996	Blackledge, Jr. et al.	395/297
☐	5689691	November 1997	Mann	395/557
☐	5727208	March 1998	Brown	395/653
☐	5740380	April 1998	LaBerge et al.	395/287

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☐	5742847	April 1998	Knoll et al.	395/866
☐	5778194	July 1998	McCombs	395/280
☐	5862369	January 1999	Parks et al.	395/558
☐	5968147	October 1999	Polfer et al.	710/52
☐	6018803	January 2000	Kardach	713/323
☐	6122693	September 2000	Gutta et al.	710/107
☐	6145040	November 2000	La Berge et al.	710/107
☐	6163824	December 2000	Quackenbush et al.	710/100
☐	6266723	July 2001	Ghodrat et al.	710/100
☐	6295568	September 2001	Kelley et al.	710/305
☐	6425079	July 2002	Mahmoud	713/2

OTHER PUBLICATIONS

U.S. Pending patent application Ser. No. 09/637,039 entitled "System and Method for Cabling Computing Equipment" filed by Hsieh et al and assigned to Dell Products L.P. (DC-02474) filed Aug. 10, 2000.
U.S. Pending patent application Ser. No. 09/637,645 entitled "A System and Method for Virtual Setup and Configuration for a Build-to-Order Computer" filed by Eynon et al. and assigned to Dell Products L.P. (DC-02378) filed Aug 14, 2000.

ART-UNIT: 2111

PRIMARY-EXAMINER: Dang; Khanh

ATTY-AGENT-FIRM: Baker Botts L.L.P.

ABSTRACT:

A system and method are provided for configuring an I/O bus. The system and method includes a plurality of adapter cards. A plurality of adapter card slots associated with the I/O busses receive the adapter cards into the computer. A user initiates optimization to check for configuration optimization problems and more specifically to check the placement of the adapter cards within the adapter card slots of the I/O busses. The user initiates optimization and in turn activates the improvement engine within the computer. The improvement engine analyzes the data transfer rates of the I/O busses and adapter cards and the placement of the adapter cards to determine an improved configuration of the adapter cards within the I/O busses. Indicators located proximate to the I/O busses display visual indication regarding the adapter card placement within the I/O busses allowing the user to determine if the configuration can be improved.

23 Claims, 4 Drawing figures

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L3: Entry 4 of 6 File: USPT Apr 4, 2000

DOCUMENT-IDENTIFIER: US 6047379 A
TITLE: Information bus regenerator

Detailed Description Text (3):
Referring in particular to FIGS. 3 and 4, the bus regenerator 6 shown has a housing 8 and two sockets 10 and 13 on opposite ends of housing 8, and status indicator light emitting diodes ("LEDs") 14. Sockets 10 and 13 are female sockets of identical 68 pin configuration for wide SCSI bus connection, with socket 13 being for connection to a differential SCSI bus, and therefore include pins connected to a number of data and control lines as well as at least one termination power line. Sockets 10 and 3 each can repetitively and releasably engage and disengage with mating male socket members 60 and 82, respectively, by manual insertion/removal in a known manner. Optional additional mating screw/threaded bore fasteners (not shown) can secure any one of sockets 10, 13 and its engaged mating socket member in the engaged position. An active terminator unit 14, and a passive terminator unit 18, both of known configuration, are connected to respective sockets 10 and 13 to terminate each of the data and control lines from a connected bus, in a known manner. Active terminator unit 14 includes three active terminator ICs, such as those made by Linfinity (Garden Grove, Calif.).

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L3: Entry 4 of 6 File: USPT Apr 4, 2000

US-PAT-NO: 6047379
DOCUMENT-IDENTIFIER: US 6047379 A

TITLE: Information bus regenerator

DATE-ISSUED: April 4, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Larabell; Henri J.	San Jose	CA		
Kiesselbach; Kevin	San Carlos	CA	94070	

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Larabell; Henri	San Jose	CA			04
Kiesselbach; Kevin	San Carlos	CA			04

APPL-NO: 08/ 991993 [PALM]
DATE FILED: December 17, 1997

INT-CL: [07] G06 F 1/26, G06 F 13/40, H01 P 1/24

US-CL-ISSUED: 713/300; 326/30, 710/101, 307/66
US-CL-CURRENT: 713/300; 307/66, 326/30

FIELD-OF-SEARCH: 713/300, 710/100, 710/101, 710/2, 307/66, 326/86, 326/30, 333/22R, 361/683, 327/530

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4015147	March 1977	Davidson et al.	327/566
☐	4604689	August 1986	Burger	364/200
☐	5208562	May 1993	Schirm, IV	333/22R
☐	5337413	August 1994	Lui et al.	395/275
☐	5495584	February 1996	Holman, Jr. et al.	395/308
☐	5577205	November 1996	Hwang et al.	395/200.01

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☐	5596757	January 1997	Smith	395/750
☐	5680065	October 1997	Park	326/86
☐	5754868	May 1998	Yamamoto et al.	713/300
☐	5864715	January 1999	Zani et al.	710/63

ART-UNIT: 271

PRIMARY-EXAMINER: Ray; Gopal C.

ATTY-AGENT-FIRM: Chaikin; Douglas A. Peninsula IP Group

ABSTRACT:

A bus regenerator, and an extended bus information system and method of communicating information, using such a regenerator. A bus regenerator has first and second information buses. A processor is connected to transfer information between the buses and at least one terminator is connected to terminate one of the buses (preferably a terminator is provided for each bus). A termination power line supplies termination power to the terminator and power to the processor. Additionally, a rechargeable power source, particularly a rechargeable battery, is connected to the termination power line, so as to supply power to at least one of the terminator and the processor, and recharge from the termination power line, as total power used by the terminator and processor varies.

33 Claims, 9 Drawing figures

US006754747B2

(12) **United States Patent**
Locklear et al.

(10) **Patent No.: US 6,754,747 B2**
(45) **Date of Patent: Jun. 22, 2004**

(54) **SYSTEM AND METHOD FOR CONFIGURING AN I/O BUS**

(75) Inventors: **David A. Locklear**, Austin, TX (US); **Michael A. Wright**, Round Rock, TX (US)

(73) Assignee: **Dell Products L.P.**, Round Rock, TX (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 479 days.

(21) Appl. No.: **09/769,799**

(22) Filed: **Jan. 25, 2001**

(65) **Prior Publication Data**

US 2002/0099875 A1 Jul. 25, 2002

(51) **Int. Cl.**[7] **G06F 13/00**
(52) **U.S. Cl.** **710/100**; 710/107
(58) **Field of Search** 710/47, 33–52, 710/57, 58, 109, 100, 107, 113, 154, 323, 305; 713/2, 600

(56) **References Cited**

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OTHER PUBLICATIONS

U.S. Pending patent application Ser. No. 09/637,039 entitled "System and Method for Cabling Computing Equipment" filed by Hsieh et al and assigned to Dell Products L.P. (DC–02474) filed Aug. 10, 2000.

U.S. Pending patent application Ser. No. 09/637,645 entitled "A System and Method for Virtual Setup and Configuration for a Build–to–Order Computer" filed by Eynon et al. and assigned to Dell Products L.P. (DC–02378) filed Aug 14, 2000.

* cited by examiner

Primary Examiner—Khanh Dang
(74) *Attorney, Agent, or Firm*—Baker Botts L.L.P.

(57) **ABSTRACT**

A system and method are provided for configuring an I/O bus. The system and method includes a plurality of adapter cards. A plurality of adapter card slots associated with the I/O busses receive the adapter cards into the computer. A user initiates optimization to check for configuration optimization problems and more specifically to check the placement of the adapter cards within the adapter card slots of the I/O busses. The user initiates optimization and in turn activates the improvement engine within the computer. The improvement engine analyzes the data transfer rates of the I/O busses and adapter cards and the placement of the adapter cards to determine an improved configuration of the adapter cards within the I/O busses. Indicators located proximate to the I/O busses display visual indication regarding the adapter card placement within the I/O busses allowing the user to determine if the configuration can be improved.

US005878238A

United States Patent [19]

Gan et al.

[11] Patent Number: 5,878,238

[45] Date of Patent: Mar. 2, 1999

[54] **TECHNIQUE FOR SUPPORTING SEMI-COMPLIANT PCI DEVICES BEHIND A PCI-TO-PCI BRIDGE**

[75] Inventors: **Doron Gan**; **Jeff Savage**, both of Austin, Tex.

[73] Assignee: **Dell USA, L.P.**, Round Rock, Tex.

[21] Appl. No.: **908,650**

[22] Filed: **Aug. 7, 1997**

Related U.S. Application Data

[62] Division of Ser. No. 590,461, Jan. 23, 1996.

[51] **Int. Cl.**[6] **G06F 1/30**; G06F 13/40

[52] **U.S. Cl.** **395/308**; 395/309; 395/828; 395/183.12

[58] **Field of Search** 395/280–284, 395/306–309, 828–834, 183.12

[56] **References Cited**

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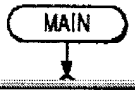
[57] **ABSTRACT**

Method and apparatus for detecting the presence of a semi-compliant PCI device in a secondary expansion slot of a PC and instructing the user to reinsert the device into one of the primary slots are disclosed. In one embodiment, upon detection of a semi-compliant PCI device in a secondary slot, a video image instructing the user to reinsert the device into one of the primary slots is displayed on a display of the PC. Operation remains suspended until the device is relocated to a primary slot. In a presently preferred embodiment, a hardware enhancement to a PCI-to-PCI bridge connecting a primary PCI bus to a secondary BCI bus enables the device to operate flawlessly on the secondary PCI bus, such that the user remains unaware of the otherwise undesirable situation.

24 Claims, 2 Drawing Sheets



US-PAT-NO: 5790814

DOCUMENT-IDENTIFIER: US 5790814 A

TITLE: Technique for supporting semi-compliant PCI devices behind a PCI-to-PCI bridge

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Detailed Description Text - DETX (2):

As described above, FIG. 1 is a system block diagram of a PC 10 comprising a conventional PCI bus configuration. Referring now to FIGS. 2A and 2B, a flowchart of a method of detecting the presence of a semi-compliant PCI device in a secondary expansion slot and informing the user of this condition via a video image or other indicator. In particular, the method illustrated in FIGS. 2A and 2B utilizes an exception handler to detect that a semi-compliant PCI device is plugged into one of the secondary slots 36a-36c and instruct the user to move the device from the secondary slot to one of the primary slots 28a, 28b. It will be appreciated that instructions for execution by the host processor for implementing the method illustrated in FIGS. 2A and 2B, as well as the method illustrated in FIG. 3, are stored in a memory device of the PC 10.

First Hit Fwd Refs

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L1: Entry 1 of 1 File: USPT Mar 11, 1997

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TITLE: Computer system modular add-in daughter card for an adapter card which also functions as an independent add-in card

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